Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 15 (Canceled)

Claim 16 (new)

An internal switching fabric within an System-on-Chip (SOC) that routes signals between requestors and addressable targets, comprising:

one or more requestor connection ports that couple to one or more requestors;

one or more target connection ports that couple to one or more addressable targets wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system;

one or more decoder/router elements that couple to said requestor connection ports and said target connection ports, said decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target;

wherein one of said one or more decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets; and

wherein additional said requesters may be coupled to the internal switching fabric adding additional said requestor connection ports.

Claim 17 (new)

The claim of claim 16 further comprising one or more arbiters one that couple to said decoder/router elements and arbitrates said requests between said requestor connection ports and said target connection ports to said designated target.

Claim 18 (new)

The claim of claim 16 wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port.

Claim 19 (new)

The claim of claim 16 wherein said request routed to said designated target by said decoder/router element further comprises a registered, point-to-point signal that further comprises a plurality of pipeline stages.

Claim 20 (new)

An method to manufacture an internal switching fabric within an System-on-Chip (SOC) that routes signals between requestors and addressable targets, comprising:

coupling one or more requestor connection ports to one or more requestors;

coupling one or more target connection ports to one or more addressable targets wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system;

coupling one or more decoder/router elements to said requestor connection ports and said target connection ports, said decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target;

wherein one of said one or more decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets; and

wherein additional said requesters may be coupled to the internal switching fabric adding additional said requestor connection ports.

Claim 21 (new)

The claim of claim 20 further comprising one or more arbiters one that couple to said decoder/router elements and arbitrates said requests between said requestor connection ports and said target connection ports to said designated target.

Claim 22 (new)

The claim of claim 20 wherein one of said one or more requestors and one of said one or more addressable targets together further comprise a single device having an independently accessible requestor port and an independently accessible target port.

Claim 23 (new)

The claim of claim 20 wherein said request routed to said designated target by said decoder/router element further comprises a registered, point-to-point signal that further comprises a plurality of pipeline stages.

Claim 24 (new)

An internal switching fabric within an System-on-Chip (SOC) that routes signals between requestors and addressable targets, comprising:

providing one or more requestor connection ports that couple to one or more requestors;

providing one or more target connection ports that couple to one or more addressable targets wherein each said addressable target has a unique address space and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system;

providing one or more decoder/router elements that couple to said requestor connection ports and said target connection ports, said decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target;

wherein one of said one or more decoder/router elements further comprises one of the following:

a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets;

a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes